presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d (BNA) 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. (BNA) 171, 174 (C.C.P.A. 1979)). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). The Examiner can only rely on references which are either in the same field as that of the invention, or if not in the same field, the references must be "reasonably pertinent to the particular problem with which the inventor was concerned." *M.P.E.P.* § 2141.01 (a) (citing *In re Oetiker*, 24 U.S.P.Q.2d (BNA) 1443 at 1445). The Examiner must also recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d (BNA) 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990). If the proposed modification renders the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)).

The Examiner must also avoid hindsight. *Id.* The Examiner cannot use the Appellant's structure as a "template" and simply select elements from the references to reconstruct the claimed invention. *In re Gorman,* 933 F.2d 982, 987, 18 U.S.P.Q.2d (BNA) 1885, 1888 (Fed. Cir. 1991).

b) The References

Manning: teaches a memory device which can be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address.

(Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture to Manning's invention is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50). However, no details of how to apply the architecture, or its operation, are given.

Rosich: describes a dynamic random access memory (DRAM) device which uses the state of the write enable (WE) signal to select page mode or nibble mode operation at the first column address strobe (CAS) signal assertion after a row address strobe (RAS) signal assertion. (Col. 6, lines 25-28). After being placed in nibble mode, the counter enable (CEN) signal permits a counter to internally increment column addresses. (Col. 7, lines 18-21; and FIG. 5A). Pipelined operation is not discussed.

c) Discussion of the Rejections

***c.1* -- The rejection under § 102**

Claims 36-39, 59-64, 69, and 75-83 were rejected under 35 USC § 102(e) as being anticipated by Manning. First, the Appellants do not admit that Manning is prior art and reserve the right to swear behind this reference in the future. Second, the Appellants respectfully submit that a case of anticipation under 35 U.S.C. § 102(e) has not been established because Manning does not disclose each and every element of claims 36-39, 59-64, 69, and 75-83. Therefore, the Appellants respectfully traverse this rejection under 35 U.S.C. § 102(e).

c.1.1. Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.

Manning specifically fails to disclose "selecting between a burst mode and a pipelined mode of operation" as claimed by the Appellants in claim 36 or selecting a burst mode of operation or a pipeline mode of operation as claimed by Appellants in claims 63 and 68. Similarly, Manning fails to disclose the order of address access "in the pipelined mode" (claims 37, 76, and 81), or "in the burst mode" in conjunction with selecting between the burst and

pipelined modes of operation (claim 38); or "selecting at least one address pathway based on the selection between the burst mode and the pipelined mode" (claim 39).

Further, Manning fails to teach "choosing whether the memory is in a burst mode ... or in a pipeline mode of operation", "switching between the burst mode ... and the pipelined mode", "switching between ... read ... and write operation[s]" in conjunction with choosing a pipelined mode of operation, or "operations ... performed in a different order" in conjunction with choosing a pipelined mode of operation (claims 59-62).

In addition, Manning fails to describe "selecting an external address only data path ... if ... the pipelined mode of operation is selected" (claim 63), or "operations ... performed in a different order" (including selecting a pipelined mode of operation) (claim 64). Manning also fails to describe "changing [a] ... mode select signal to select a pipelined mode of operation" (claims 65 and 67), and "switching the mode of operation to a pipelined mode" (claim 66). Manning further fails to disclose "selecting an external address only data path, obtaining an external column address, and accessing the memory when the pipeline mode of operation is selected" (claim 68).

Finally, Manning fails to include any teaching of "switching from a burst mode ... to a pipelined mode" (claims 75 and 80), "selecting at least one address pathway" based upon such switching (claims 77 and 82), "subsequently switching from the pipelined mode ... to the burst mode" (claims 78 and 83), or "selecting at least one address pathway" based upon such subsequent switching (claim 79). Manning also fails to describe a storage device including mode circuitry "configured to select between a burst mode and a pipeline mode" along with "an external column address data path for pipeline read and write operation column address generation" (claim 69).

Several assertions were made in the Office Action which attribute support to various concepts allegedly disclosed by Manning. However, a careful reading of each citation reveals errors with respect to the asserted elements. These assertions have been made with respect to:

Claim 36, 60, 75, and 80 - Manning does not disclose switching or selecting between a burst mode and a pipelined mode (Manning never discusses switching or selecting between the modes, only operation in the burst mode, and the possibility of using a pipelined architecture).

Claims 37, 76, and 81 - Manning does not disclose obtaining a second external column address ... for operation in the pipeline mode (Manning merely refers to the possibility of using a pipelined *architecture*, and never discusses the details of how it might operate).

Claim 39, 77, 82 - Manning does not disclose selecting an address pathway based on ... selection between a burst mode and a pipelined mode (since Manning never discloses selecting between burst and pipelined modes in the same device).

Claims 78, 79, and 83 - Manning does not disclose, discuss, or teach switching from pipelined mode to burst mode (Manning merely refers to the possibility of using a pipelined *architecture*).

Claims 63 and 69 - Manning does not disclose an external address only path for the pipeline mode, or pipeline/burst circuitry (since Manning explains nothing about a pipelined architecture, other than generally characterizing its operation).

c.1.2. Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support *switching* or *selecting* between burst and pipelined modes of operation, as claimed in claims 36, 59, 63, 65, 66, 67, 68, 69, 75, and 80 (and in all claims that depend from them)?

Second, the Office has failed to establish a case of anticipation. While the assertion is made that Manning discloses "choosing whether the memory is in burst or a pipelined mode of operation","switching between a burst mode and a pipeline mode", and "pipeline/burst circuitry", the Appellants' representative, after a careful study of Manning, was unable to locate any such discussion, nor any such circuitry which was configurable to select or switch between burst and pipelined modes of operation.

For example, the only elements offered by the Office to support the assertion that Manning "discloses the invention as claimed" with respect to claims 36, 75, and 80 are: FIG.1

EDO signal, and FIG. 2 ADDR, ROW, COLm, and /WE signals; col. 5, lines 43-50; col. 6, lines 14-34; and col 7, lines 43-54. Fig. 1 is a block diagram of an EDO memory that operates in burst or page modes, with no indication regarding exactly which modes may be operative, or how they may be selected. Col. 5, lines 41-50 discuss the possibility of using a pipelined architecture, but not as enabling switching between pipeline mode and burst operations within the *same* memory, as disclosed and claimed by the Appellants. Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning never discusses the ability to *select* or *switch* between burst and pipelined modes of operation, or circuitry to effect such a selection, as claimed by the Appellants in independent claims 36, 59, 63, 65, 66, 67, 68, 69, 75, and 80, and all of the claims which depend from them. It should also be noted that one does not have to "select pipeline mode" to "work in the pipeline architecture," as asserted in the Office Action. For example, if a device always operates in the pipelined mode, and is unable to switch to another mode, the pipelined mode does not have to be selected.

Another way of viewing this issue is to ask the question: How can a memory have a pipelined architecture (as mentioned by Manning) without inherently operating in the pipelined mode (as claimed by the Appellants)? The brief answer is that a memory, such as a burst EDO memory, may include pipelined registers that permit the rapid generation of *internal* addresses. However, *external* addresses are still received and processed in the same fashion as regular EDO memory. See, for example, the definition for "Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999, attached hereto as Appendix II.

In memory terminology, a row of memory cells is called a page. With page-mode memory, a row address is applied to the chip and the RAS signal held active while sequential column addresses are applied and the CAS signal cycled until an entire row of memory cells are read or written. By addressing columns in this manner, all of the memory cells in a selected row can be written or read without changing the row address. Since page-mode memory requires a setup time for each column address, it was eventually replaced with fast page-mode memory.